Remarks

Applicants respectfully request that this amendment be entered, and that their subject U.S. Patent application be passed to issuance in view thereof. Applicants respectfully submit that the following amendment does not introduce new matter requiring further search by the Examiner. Independent claims 1, 11, 12, 14 and 18 have been amended to include the limitation of canceled claim 19 which was added in the amendment of June 6, 2002. The foregoing amendments are further indicated in blackline form in Exhibit A, "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Applicants respectfully request that claim 18 be amended to correct the typographical error noted by the Examiner and to address the §112, second paragraph rejection thereto.

In the Office Action, pending claims 18-19 stand rejected under 35 U.S.C. 102(b) as being anticipated by Eklund (U.S. Patent No. 5,087,580). In response, Applicants respectfully submit that Eklund neither anticipates nor suggests the invention as recited in the claims as presented herein.

Applicants respectfully request that claim 19 be canceled, and claim 18 be amended to recite the limitation of "... wherein said buried collector region and said base region are formed by implantation through **a single mask** formed on the SOI substrate." Claim 18, as amended, specifies that the two regions are formed through a **single mask**, as taught at page 7, lines 17-18. Claim 18, as amended, recites the collector disposition and collector-base stacking features of the invention as discussed at page 6, line 17 through page 7, line 11 and as shown in Fig. 1 (as well as virtually all of the remaining Figures). The significance of these features of the invention in reducing base width while reducing collector capacitance is discussed at page 7, lines 12-16.

Applicants respectfully submit that the method of forming the recited collector-base regions

using a single mask is neither anticipated nor suggested by Eklund. Eklund teaches patterning with a first mask to form the inverse of the bipolar collector region, stripping the nitride 22 and implanting to form the bipolar collector 26 (FIG. 2; column 4, lines 26-34). Then, Eklund teaches patterning with a second mask and etching to form the CMOS and bipolar mesas 13 and 11 (FIG. 3; column 4, lines 36-38). Bipolar base 48 is formed by ion implanting into bipolar mesa 11 (FIG. 5; column 4, lines 66-68). Therefore, Eklund requires at least **2 separate masks** to form the base and collector regions. Applicants invention requires only a single mask to form both regions resulting in reduced processing time and costs compared to Eklund.

Therefore, Applicants respectfully submit that the rejections under 35 U.S.C. 102(b) have been overcome.

In the Office Action, pending claims 1-5, 7-18 and 20 stand rejected under 35 U.S.C. 103 in view of various combinations of the teachings of U.S. Patent 5,087,580 ("Eklund"), U.S. Patent 5,904,536 ("Blair"), U.S. Patent 5,352,624 ("Miwa et al.") and U.S. Patent 5,406,113 ("Horie"). In response, Applicants respectfully submit that these various combinations of references neither teach nor suggest the invention as recited in the claims as presented herein.

Applicants respectfully request that independent claims 1, 11, 12, 14 and 18 be amended to make it clear that the base and collector regions are formed using a **single mask**. As discussed above, Eklund neither teaches nor suggests Applicants' recited claims as presented herein. Similarly, Blair neither teaches nor suggests Applicants' recited claims as presented herein. Blair teaches a collector 202 formed using a first mask (FIG. 2A), and a base 206 formed by a second mask (FIG. 2B). Thus, the various combinations of Eklund with Blair, Miwa et al. or Horie neither teach nor suggest Applicants' invention as recited in the claims, as amended.

Therefore, Applicants respectfully submit that the rejections under 35 U.S.C. 103(a) have been overcome.

Accordingly, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments, questions, or suggestions, please do not hesitate to contact the undersigned agent at the telephone number and/or email address set forth below.

Respectfully submitted,

For: Divakaruni et al.

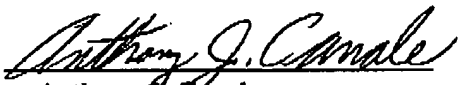
By: 

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Exhibit A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend the following claims:

1. (Twice Amended) A method of forming an emitter in a vertical bipolar transistor comprising:

providing a substrate having a collector layer and a base layer over said collector layer, said collector layer and said base layer are formed by implantation through a single mask formed on the substrate;

forming a patterned mask over said base layer; and

filling openings in said mask with emitter material in a damascene process, said emitter material contacting the substrate.

11. (Twice Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector, said collector layer and said base layer are formed by implantation through a single mask formed on the SOI substrate;

forming a gate oxide layer over only said CMOS region of said SOI substrate;

forming a polysilicon layer over a CMOS region of said SOI substrate;

patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region

depositing an emitter material in said openings in a damascene process to form emitters;

removing said mask;

patterning said polysilicon layer to form gate conductors; and

forming sidewall spacers adjacent said emitters and said gate conductors.

12. (Twice Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector, said collector layer and said base layer are formed by implantation through a single mask formed on the SOI substrate;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

14. (Twice Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector, said collector layer and said base layer are formed by implantation through a single mask formed on the SOI substrate;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors. wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

18. (Once Amended) A method of forming a bipolar device on a SOI substrate having a semiconductor layer overlying a buried insulator layer ~~that~~ to forms an interface where a surface of the semiconductor layer is adjacent to a surface of the buried insulator layer ~~with an overlying semiconductor layer~~, comprising the steps of:

forming in said semiconductor layer a buried collector region ~~centered~~ centered at approximately said interface; and

forming in said semiconductor layer a base region vertically stacked on said buried collector region;

wherein said buried collector region and said base region are formed by implantation through a single mask formed on the SOI substrate.